Government of Karnataka
Department of Technical Education
Bengaluru

	**Course Title: Computer Organization**		
	Scheme (L:T:P) : **4:0:0**	Total Contact Hours: **52**	Course Code: **15CS32T**
	Type of Course: **Lectures, Self Study & Student Activity.**	Credit **:04**	Core/ Elective: **Core**
CIE- 25 Marks			SEE- 100 Marks

Prerequisites

Fundamentals of Digital electronics and basics of Computers and its peripherals.

Course Objectives

Understand the organization of a computer with its various processing units, memory and peripherals.

Course Outcome

On successful completion of the course, the students will be able to attain below Course Outcome (CO):

Course outcome		CL	Linked PO	Teaching Hours
CO1	Recognize and explain the functional units of computers	***R***	**1,2,10**	**02**
CO2	Describe assembly languages and machine instructions by analyzing how the data is stored and fetched from memory.	***U, A***	**1,2,3,4,8,10**	**10**
CO3	Explain the execution of complete instruction and bus organizations.	***U***	**2,8,9,10**	**08**
CO4	Identify various interrupt handling mechanism and buses.	***U, A***	**1,2,3,8,9,10**	**10**
CO5	Differentiate between different types of memories.	***U, A***	**1,2,3,4,5,6,7,8,9,10**	**14**
CO6	Discuss core architecture and pipelined concept.	***U***	**2,10**	**08**
		Total sessions		**52**

Legends: R = Remember U= Understand; A= Apply and above levels (Bloom's revised taxonomy)

Course-PO Attainment Matrix

Course	Programme Outcomes									
	1	2	3	4	5	6	7	8	9	10
Computer Organisation	**3**	**3**	**2**	**2**	**1**	**1**	**1**	**3**	**3**	**3**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3

If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2

If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1

If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.

Course Content and Blue Print of Marks for SEE

Unit No	Unit Name	Hour	Questions to be set for SEE			Marks Weightage	Marks Weightage (%)
			R	U	A	A	
I	Basic Structure Of Computers	**02**	5	-	-	5	4
II	Machine Instructions and Programs	**10**	-	20	8	28	18
III	Basic Processing Unit	**08**	-	22	-	22	15
IV	Input/Output Organization	**10**	-	18	10	28	18
V	The Memory system	**14**	-	20	18	38	30
VI	Processors and Pipelining	**08**	-	24	-	24	15
	Total	**52**	**5**	**104**	**36**	**145**	**100**

UNIT I : Basic Structures of Computers 02 Hrs

Functional Units, Input Unit, Memory Unit, Arithmetic and Logic Unit, Output Unit, Control Unit, Basic Operational Concepts, Bus Structures.

UNIT II: Machine Instructions & Programmes 10 Hrs

Memory Locations and Addresses , Byte Addressability, Big Endian and Little Endian Assignments, Word Alignment, Accessing numbers, characters and character strings, Memory Operations, Instruction and Instruction sequencing, Register Transfer notation, Assembly Language notation, Basic instruction types, Instruction execution and straight line sequencing, Branching, Condition codes, Addressing modes, Implementation of variables and constants, Indirection and pointers, Indexing and arrays, Relative addressing, Additional modes, Assembly Language, Assembler directives, Assembly and execution of programs, Basic Input- Output Operations.

UNIT III: Basic Processing Unit 08 Hrs

Some Fundamental Concepts, Register transfers, Performing an Arithmetic or Logic operation, Fetching a word from memory, Storing a word in memory, Execution of a complete Instruction, Branch instructions, Multiple Bus Organization, Hardwired

Control(basic block diagram only), A complete processor, Basic organization of Micro programmed Control Unit.

UNIT IV: Input Output Organization 10 Hrs

Accessing I/O Devices, Interrupts, Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device requests, Exceptions, Direct Memory Access, Bus arbitration, Buses, Synchronous bus, Asynchronous bus, Interface Circuits, Parallel port and Serial port (Basic concept only), Standard I/O Interfaces (Basic concepts only), Peripheral Component Interconnect (PCI) Bus , SCSI Bus(Basic concepts only), Universal Serial Bus (USB) (Basic concepts only)

UNIT V: The Memory System 14 Hrs

Some Basic Concepts, Semiconductor RAM Memories, Internal Organization of memory chips, Static Memories, Asynchronous DRAMs, Synchronous DRAMs, Structure of larger memories, Memory system consideration, Rambus memory, Read-Only Memories- ROM, PROM, EPROM, EEPROM, Flash Memory, Speed, Size and Cost, Cache Memories...

UNIT VI: Processors and Pipelining 08 Hrs

Processor- Introduction, Advanced processor technology, instruction set architectures, CISC scalar processor, RISC scalar processor, comparison CISC and RISC, super scalar processor (basic concept only), VLIW architecture, comparison of super scalar and VLIW, Multi core architecture
Pipelining- Introduction, pipeline principles-linear pipeline processor-Asynchronous model, synchronous model, Non linear pipeline processor, classification of pipeline processor

Text Books

1. Computer Organization, Carl Hamacher, zvonko Vranesic and Safwat Zaky, McGraw Hill, 5th edition **(Chapters 1, 2, 4, 5, 7, for UNIT I to UNIT V)**

2. Advanced Computer Architecture (A practical approach), Rajiv Chopra, S. Chand, Revised edition, reprint 2014, ISBN8121930774 - for *UNIT VI page no 133 to 138 , 143 to 145 , 192 to 194 , 218 to 219 , 221 to 223*

References

1. http://elearning.vtu.ac.in/06CS46.html
2. http://nptel.ac.in/courses/Webcourse-contents/IIT-%20Guwahati/comp_org_arc/web/
3. William Stallings, “Computer Organization and Architecture: Designing for Performance”, Eighth Edition, Pearson.
4. Computer architecture and organization , 4th edition , P Chakraborty , JAICO publishers
5. http://www.srmuniv.ac.in/downloads/computer_architecture.pdf
6. http://www.dauniv.ac.in/downloads/CArch_PPTs/CompArchCh06L01PipeLine.pdf

Suggested list of student activities

Note: The following activities or similar activities for assessing CIE (IA) for 5 marks (Any one)

Student activity like mini-project, surveys, quizzes, etc. should be done in group of 3-5 students.

1. Each group should do any one of the following type activity or any other similar activity related to the course and before conduction, get it approved from concerned course co-ordinator and programme co-ordinator
2. Each group should conduct different activity and no repeating should occur.

1	Conduct a survey on various types of processors available with their features and submit a report.
2	List out the features of 8086 microprocessor and 8051 micro controller with respect to architecture and working.
3	Submit a report on hardware and software interrupts.
4	A Case study on Moore's Law about the processors and submit a report.
5	Conduct a survey on types of memories and also about the cost and speed of various memories with comparison.

Course Delivery

The course will be delivered through lectures and Power point presentations/ Video

Course Assessment and Evaluation Scheme

Method	What		To whom	When/Where (Frequency in the course)	Max Marks	Evidence collected	Course outcomes
Direct Assessment	CIE	IA	Students	Three IA tests (Average of three tests will be computed)	20	Blue books	1 to 6
				Student activity	05	Report	1 to 6
				Total	**25**		
	SEE	End Exam		End of the course	100	Answer scripts at BTE	1 to 6
Indirect Assessment	Student Feedback on course		Students	Middle of the course		Feedback forms	1,2,3 Delivery of course
	End of Course Survey			End of the course		Questionnaires	1 to 6 Effectiveness of Delivery of instructions & Assessment Methods

Note: I.A. test shall be conducted for 20 marks. Average marks of three tests shall be rounded off to the next higher digit.

Questions for CIE and SEE will be designed to evaluate the various educational components (Bloom's taxonomy) such as:

Sl. No	Bloom's Category	%
1	Remembrance	10
2	Understanding	50
3	Application	40

Note to IA verifier*: *The following documents to be verified by CIE verifier at the end of semester

1. Blue books (20 marks)
2. Student suggested activities report for 5 marks
3. Student feedback on course regarding Effectiveness of Delivery of instructions & Assessment Methods.

FORMAT OF I A TEST QUESTION PAPER (CIE)

Test/Date and Time	Semester/year	Course/Course Code	Max Marks
Ex: I test/6 th weak of sem 10-11 Am	I/II SEM		20
	Year:		
Name of Course coordinator : CO's:____			Units:__

Question no	Question	MARKS	CL	CO	PO
1					
2					
3					
4					

Note: Internal Choice may be given in each CO at the same cognitive level (CL).

MODEL QUESTION PAPER (CIE)

Test/Date and Time	Semester/year	Course/Course Code	Max Marks
Ex: I test/6 th weak of sem 10-11 AM	III SEM	Computer Organization	20
	Year: 2015-16	Course code:15CS32T	
Name of Course coordinator : Units:1,2 Co: 1,2			

Note: Answer all questions

Question no	Question		CL	CO	PO
1	Describe the role of MAR, MDR , PC and IR.	(5)	R	1	1,2
2	Explain the role of buffer registers	(5)	R	1	1,2
3	Describe the Big-endian and Little-endian addressability	(5)	U	2	1,2
4	Explain straight line sequencing OR Describe register and absolute addressing mode.	(5)	U	2	1,2

Format for Student Activity Assessment

DIMENSION	Unsatisfactory 1	Developing 2	Satisfactory 3	Good 4	Exemplary 5	Score
Collection of data	Does not collect any information relating to the topic	Collects very limited information; some relate to the topic	Collects some basic information; refer to the topic	Collects relevant information; concerned to the topic	Collects a great deal of information; all refer to the topic	3
Fulfill team's roles & duties	Does not perform any duties assigned to the team role	Performs very little duties	Performs nearly all duties	Performs all duties	Performs all duties of assigned team roles with presentation	4
Shares work equally	Always relies on others to do the work	Rarely does the assigned work; often needs reminding	Usually does the assigned work; rarely needs reminding	Does the assigned job without having to be reminded.	Always does the assigned work without having to be reminded and on given time frame	3
Listen to other Team mates	Is always talking; never allows anyone else to speak	Usually does most of the talking; rarely allows others to speak	Listens, but sometimes talk too much	Listens and contributes to the relevant topic	Listens and contributes precisely to the relevant topic and exhibit leadership qualities	3
					TOTAL	**13/4=3.25=4**

All student activities should be done in a group of 4-5 students with a team leader.

Diploma in Computer science & Engineering

III- Semester

Course Title: Computer Organization

Time: **3 Hours** Max Marks**: 100**

PART-A

Answer any SIX questions. Each carries 5 marks. 5X6=30 Marks

1) Explain the basic functional unit of a Computer.
2) Describe register and absolute addressing mode.
3) Write a note on register transfers.
4) Explain the concept of micro programmed control .
5) Explain how to enable and disable an interrupt.
6) Explain the use of PCI bus in the computer system.
7) Explain the Double-data-rate SDRAM concept.
8) Explain the concept of flash drives.
9) Compare super scalar verses VLIW.

PART-B

Answer any SEVEN full questions each carries 10 marks. 10X7=70 Marks

1. 1. Explain with examples one-address, two-address and three-address instruction types.
2. Describe program-controlled I/O operation.
3. Illustrate with diagram arithmetic and logic operation.
4. Describe the working of DMA.
5. Explain the serial port interface.
6. Explain the operation asynchronous DRAM.
7. Describe the features of PROM, EPROM and EEPROM.
8. Illustrate with diagram memory hierarchy with respect to speed, size and cost.
9. Explain CISC scalar and RISC scalar processor.
10. Describe Arithmetic, Instruction and processor pipelining.

MODEL QUESTION BANK

Diploma in Computer Science & Engineering

III Semester

Course Title: Computer Organization

CO	Question	CL	Marks
I	Explain the basic functional unit of a Computer.	R	05
	Describe the role of MAR, MDR , PC and IR.	R	
	Explain in brief the basic operation concept between processor and the memory.	R	
	Explain the significance of single bus structure.	R	
	Explain the role of buffer registers.	R	
II	Explain byte addressability.	U	05
	Describe the Big-endian and Little-endian addressability.	U	
	Explain the basic memory operation.	U	
	Explain straight line sequencing.	U	
	Write a note on conditional codes.	U	
	Describe register and absolute addressing mode.	U	
	Write a note on relative addressing.	U	
	Explain with examples one-address, two-address and three-address instruction types.	U	10
	Illustrate Branching concept with Example.	A	
	Illustrate with examples Indirect addressing.	A	
	Describe Indexed addressing with examples.	A	
	Explain different assembler directives.	U	
	Explain the execution of assembly language program.	U	
	Describe program controlled I/O operation.	U	
	Explain the significance of auto-increment and auto-decrement addressing mode	U	
III	Explain the different phases for instruction execution .	U	05
	Write a note on register transfers.	U	
	Explain how a complete instruction is executed.	U	
	Write a note on Hardwired control unit.	U	
	Explain the concept of micro programmed control unit.	U	
	Explain single bus organization.	U	10
	Illustrate with diagram arithmetic and logic operation.	U	
	Describe fetching a word from memory.	U	
	Explain multiple bus organization.	U	
	With block diagram explain complete processor.	U	
	Explain the memory-mapped I/O concept.	U	05
	Illustrate program controlled I/O.	U	
	Write a note on interrupts.	U	
	Explain how to enable and disable an interrupts.	U	
	Write a note on vectored interrupts.	U	
	Explain the exception concepts with respect to I/O.	U	

IV	Explain bus arbitration logic.	U	
	List the activities of an I/O interface.	U	
	Explain the use of PCI bus in the computer system.	A	
	Write a note on SCSI bus.	A	
	Explain the universal serial bus concept.	U	
	Illustrate with examples interrupt service routine.	A	10
	Explain implementation of prioritized interrupts.	U	
	Describe the working of DMA.	U	
	Explain synchronous and asynchronous bus.	U	
	Explain with example parallel port connectivity.	A	
	Explain serial port interface.	A	
V	Illustrate how to implement a static RAM memory cell.	A	05
	Illustrate how to implement CMOS memory.	A	
	Explain the Double-data-rate SDRAM concept.	U	
	Write a note on Ram bus memory.	U	
	Explain the configuration of ROM cell.	U	
	Write a note on flash memory.	A	
	Explain the concept of flash drives.	A	
	Explain the significance of cache memory.	U	
	Explain the internal organization of memory chips.	U	10
	Explain the operation of asynchronous DRAM.	U	
	Explain the operation of synchronous DRAM.	U	
	Explain static and dynamic memory system.	U	
	Explain the use of memory controller with diagram.	A	
	Describe types of ROM	A	
	Illustrate with diagram memory hierarchy with respect to speed, size and cost	U	
	Explain the working of cache memory operations.	U	
VI	Explain Architecture of RISC machine.	U	05
	Compare CISC verses RISC.	U	
	Explain super scalar processor.	U	
	Compare super scalar verses VLIW.	U	
	List advantages of multi core architecture.	U	
	List the applications of multi core architecture.	A	
	Explain Non-linear pipeline processor.	U	
	Explain VLIW Architecture.	U	10
	Explain CISC scalar and RISC scalar processor .	U	
	With neat diagram explain Multi core architecture.	U	
	Explain Asynchronous and synchronous model of linear pipeline processor.	U	
	Describe Arithmetic, Instruction and processor pipelining.	U	