Government of Karnataka
Department of Technical Education
Board of Technical Examinations, Bengaluru

Course Title :**Digital Electronics Lab – I**		Course Code	: **15EC23P**
Semester	: **II**	Course Group	: **Core**
Teaching Scheme in Hr. (L:T:P)	: **0:2:4**	Credits	: **3**
Type of course	: **Tutorial + Practical**	Total Contact Hours	: **78**
CIE	: **25 Marks**	SEE	: **50 Marks**

Prerequisites

Knowledge of basic electrical and electronics engineering in Semester-I.

Course Objectives

Learn and understand the basics of digital electronics, Boolean algebra, and able to design the simple logic circuits and test/verify the functionality of the logic circuits.

Course Outcomes

At the end of the course, the students will be able to

1. Distinguish between analog and digital systems.
2. Identify the various digital ICs and understand their operation.
3. Apply Boolean laws and K-map to simplify the digital circuits.
4. Understand the function of elementary digital circuits under real and simulated environment.
5. Prepare a report on basics of digital electronics and handling of ICs.

Course Outcome		CL	Experiments linked	Linked PO	Teaching Hrs
CO1	Distinguish between analog and digital systems.	***R/U/A***	Unit 1, Expts 1	1,2	06
CO2	Identify the various digital ICs and understand their operation.	***R/U/A***	Unit 1, Expts 2 to 3	1,2,3,10	06
CO3	Apply Boolean laws and K-map to simplify the digital circuits.	***R/U/A***	Unit 1, Expts 4 to 9	1,2,3,4,5,8 ,10	18
CO4	Understand the function of elementary digital circuits under real and simulated environment.	***U/A***	Unit 1, Expts 10 to 18	1,2,3,4,5,8 ,10	27
CO5	Prepare a report on basics of digital electronics and handling of ICs.	***U/A***	UNIT 2	1,2,3,4,5,8 ,9,10	15
		Total sessions include two tests			**78**

Course-Po Attainment Matrix

Course	Programme Outcomes									
	1	2	3	4	5	6	7	8	9	10
Digital Electronics Lab – I	**3**	**3**	**3**	**3**	**3**	**--**	**--**	**3**	**1**	**3**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3

If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2

If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1

If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.

Course Contents

UNIT – I: Tutorial and Practice Duration: 63Hr.

Sl. No.	Topic/Exercises	Duration (Hr.)
1	a) Discuss the concept of digital electronics. b) Binary systems and logic levels, TTL digital ICs, digital IC signal levels and IC numbering. c) Identify the different parts of the digital trainer kit, precautions to be followed in handling ICs, learn to identify the pins, fix the ICs and measure the voltage levels on the kit.	6
2	Explain need of logic gates, logic function, truth table, pin diagram, identify the logic gates using standard and IEEE/ANSI symbols for the NOT, 2-input OR, AND gates and observe the output.	3
3	Explain logic function, truth table, pin diagram, identify the logic gates using standard and IEEE/ANSI symbols for the NOR, NAND and EX-OR gates and observe the output.	3
4	State De Morgan's theorems and construct the simple circuits to observe their validity.	3
5	State and describe the Boolean identities and laws. Show the verification of commutative, associative and distributive Boolean laws using suitable logic gates.	3
6	Discuss the universality of NAND gates. Construct NOT, OR, AND, NOR, EX-OR and EX-NOR gates using NAND gates and show the output.	3
7	Discuss the universality of NOR gates. Construct NOT, OR, AND, NOR, EX-OR and EX-NOR gates using NOR gates and show the output.	3
8	Solve the given Boolean equations using Boolean laws and deduce the truth table and circuit for the reduced equation and show the output. a) $\overline{\overline{A} + \overline{B}}$ b)$\overline{\overline{\overline{ABC}}}$ c) $\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C}$+A$\bar{B}\bar{C}$+ AB$\bar{C}$.	3
9	Explain K-map for three and four variables, identification of pairs, quads and octets and solving sum-of-products equations. Reduce a) $\bar{A}\,\bar{B}C +$	3

	$\bar{A}B\bar{C}+A\bar{B}\bar{C}+A\bar{B}C$. b) $AB\bar{C}\bar{D} + AB\bar{C}D + ABCD + ABC\bar{D} + \bar{A}BCD + \bar{A}BC\bar{D}$ and construct the circuit and show the output	
10	Discuss binary number system, convert decimal to binary number system and vice versa, give examples to add binary numbers. Construct a truth table to add two bits showing the sum and carry results and implement the resulting half-adder using suitable logic gates.	3
11	Construct a truth table to add two bits along with a possible carry out showing the sum and carry results. Write sum-of-products equation for the output, reduce using K-map and implement the resulting full-adder using suitable logic gates.	3
12	Discuss binary subtraction. Write the truth-table for full-subtractor. Write sum-of- products equation for the output, reduce using K-map and implement using suitable logic gates.	3
13	Understand ones and two's complement arithmetic of binary numbers and their role in binary arithmetics with examples. Construct the circuit to implement the subtraction and addition of two 4-bit data using IC 7483 using two's complement method (use IC 7483 and IC 7486) and show the output.	3
14	Discuss Gray and BCD codes. Develop Binary-to-Gray code converter using IC 7486 and verify the output.	3
15	Develop Gray-to-binary code converter using IC 7486 and verify the output.	3
16	Define a parity bit. Discuss even parity and odd parity bit and its importance in communication. Develop a parity generator and checker using IC 7486.	3
17	Discuss the importance of comparator. Verify the truth table of 2-bit magnitude comparator using IC 7485.	3
18	Discuss the significance of enable/disable circuits. Demonstrate an enable/disable circuit using AND/OR, NAND/NOR gates.	3
	Two internal Assessment Test	6
	Total	**63**

UNIT – II: Project Activities [CIE- 05 Marks] Duration: 15 Hr.

Sl. No.	Activity	Duration (Hr.)
1	Collect the information about any three digital systems and highlight the difference between analog and digital systems.	**3**
2	Write a chart to represent decimal numbers from 0 to 50 in binary, octal and hexadecimal number systems.	**3**
3	Collect the information on signed and unsigned binary numbers. Prepare a chart to represent the decimal numbers from -20 to +20 in 8-bit format in signed and singned-magnitude representation.	**3**
4	Perform binary multiplication and division with examples.	**3**
5	List the features of BCD, ASCII excess-3 codes with examples.	**3**
6	Open-ended activity like (i) Simulate a realistic digital circuit containing at least six logic gates. (ii) Collect the catalogues and specification sheets or a chart displaying various logic ICs (At least 10). (iii) Record the best practices used in the disposal of e-waste and	

	precautions in the operation of digital systems. (iv) Any other such activities that can contribute for the student's knowledge in respect of this course.	

Execution Mode

1. Maximum of 2 students in each batch for project activity.
2. Project activity 1 to 5 compulsory (handwritten) and 6 are mandatory for every batch.
3. Project activities shall be carried out throughout the semester and present the project report at the end of the semester.
4. Write qualitative report not exceeding 10 pages; one report per batch.
5. Each of the activity can be carried out off-class; however, demonstration/presentation should be done during laboratory sessions.
6. Assessment shall be made based on quality of activity, presentation/demonstration and report.

References

1. *Digital Principles and Applications*, Donald P Leach, Albert Paul Malvino,Goutam Saha,McGraw-Hill publications.
2. *Digital Systems Principles and Applications*, Ronald J.Tocci,Neal S Widmer,Gregory L.Moss. Pearson Publication.
3. http://www.vlab.co.in/
4. http://www.asic-world.com/
5. http://www.vlab.co.in/
6. http://electrical4u.com/
7. http://www.electronics-tutorials

Course Delivery

The course will be delivered through two-hour tutorials and four-hour hands-on practice per week

Course Assessment and Evaluation Scheme

Method	What		To whom	When/Where (Frequency in the course)	Max Marks	Evidence collected	Course Outcomes
DIRECT ASSESSMENT	CIE (Continuous Internal Evaluation)	IA Tests	Students	Two IA Tests(Average of two tests will be computed)	10	Blue books	1 to 5
				Record Writing(Average of Marks allotted for each experiment)	10	Record Book	1 to 5
				Mini Project	05	Report/Model	1 to 5
				Total	25		
	SEE (Semester End Examination)	End Exam		End of the course	50	Answer scripts at BTE	1 to 5
INDIRECT ASSESSMENT	Student Feedback on course		Students	Middle of the course		Feedback forms	1 to 3 Delivery of course
	End of Course Survey			End of the course		Questionnaires	1 to 5 Effectiveness of Delivery of instructions & Assessment Methods

***CIE** – Continuous Internal Evaluation ***SEE** – Semester End Examination

Note:

1. I.A. test shall be conducted as per SEE scheme of valuation. However obtained marks shall be reduced to 10 marks. Average marks of two tests shall be rounded off to the next higher digit.
2. Rubrics to be devised appropriately by the concerned faculty to assess Student activities.

MODEL OF RUBRICS FOR ASSESSING STUDENT ACTIVITY

Dimension	Scale					Students exam Reg no/ Score				
	1.Unsatisfactory	2.Developing	3.Satisfactory	4.Good	5.Exemplary	Reg1	Reg2	Reg3	Reg4	Reg5
1.Research and gather information	Does not collect information relate to topic	Collects very limited information, some relate to topic	Collects basic information, most refer to the topic	Collects more information, most refer to the topic	Collects a great deals of information, all refer to the topic	3				
2.Full fills teams roles and duties	Does not perform any duties assigned to the team role	Performs very little duties	Performs nearly all duties	Performs almost all duties	Performs all duties of assigned team roles	2				
3.Shares work equality	Always relies on others to do the work	Rarely does the assigned work, often needs reminding	Usually does the assigned work, rarely needs reminding	Always does the assigned work, rarely needs reminding.	Always does the assigned work, without needing reminding	5				
4.listen to other team mates	Is always talking, never allows anyone to else to speak	Usually does most of the talking, rarely allows others to speak	Listens, but sometimes talk too much,	Listens and talks a little more than needed.	Listens and talks a fare amount	3				
					Total Marks	13/4=3.25=04				

Composition of Educational Components

Questions for CIE and SEE will be designed to evaluate the various educational components such as shown in the following table.

Sl. No.	Component	Weightage (%)
1	Remembering and Understanding	25
2	Applying the knowledge acquired from the course	35
3	Analysis	40

Scheme of Evaluation for Semester End Exam

Sl. No.	Scheme	Max. Marks
1	Write-up for theory questions	10
2	Writing circuit and procedure of one experiment	10
3	Conduction	15
4	Result	05
5	Viva-voce	10
TOTAL		**50**

Note:
1. Candidate shall submit Lab record for the examination.
2. Student should be allowed to conduct directly even if she/he is unable to write the procedure.

Laboratory Resource Requirements

Hardware Requirement:For a batch of 20 students

Sl. No.	Equipment	Quantity
1	Digital trainers	15
2	Dual trace oscilloscope.	05
3	Digital multimeters	05
4	ICS-7400,7402,7404,7408,7432,7486,7483,7485,7427	10 each
5	Patch cards(different lengths)	250
6	Digital IC Tester	02
7	Logic Pulser	02

Model Questions for Practice and Semester End Examination

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N**ote:** The questions in the question bank are indicative but not exhaustive.

1. Write Truth table and show the outputs of 2-input OR, AND, NOR gates using suitable TTL ICs.
2. Write the truth table and show the outputs of NOT gate, 2-input NAND, EX-OR gates using suitable TTL ICs.
3. Construct the circuit to verify De-Morgan's theorems and show the results.
4. Construct the circuit to show that NAND gate is equivalent to bubbled OR- gate.
5. Construct the circuit to show that NOR gate is equivalent to bubbled AND- gate.
6. Construct the circuit to verify the equation $\overline{A+B} = \bar{A}\bar{B}$
7. Construct the circuit to demonstrate commutative, associative Boolean laws using suitable logic gates.
8. Construct the circuit to demonstrate commutative and distributive Boolean laws using suitable logic gates.
9. Construct the circuit to demonstrate associative and distributive Boolean laws using suitable logic gates.
10. Construct NOT, OR, AND gates using NAND gates and show the verification of the truth table.
11. Construct NOT, AND, NOR gates using NAND gates and show the verification of the truth table.
12. Construct NOT and EX-OR gates using NAND gates and show the verification of the truth table.
13. Construct AND and EX-NOR gates using NAND gates and show the verification of the truth table.
14. Construct NOT, OR, AND gates using NOR gates and show the verification of the truth table.
15. Construct NOT, AND, NAND gates using NOR gates and show the verification of the truth table.
16. Construct NOT and EX-OR gates using NOR gates and show the verification of the truth table.
17. Construct OR and EX-NOR gates using NOR gates and show the verification of the truth table.
18. Construct using suitable gates to show the verification of AB+A$\bar{B}$ =A
19. Construct using suitable gates to show the verification of A+$\bar{A}$B=A+B.
20. Construct using suitable gates to show the verification of A+$\bar{A}$ = 1.
21. Construct using suitable gates to show the verification of A.$\bar{A}$ =0
22. Solve the given Boolean equations using Boolean laws and deduce the truth table and circuit for the reduced equation and show the output. a) $\overline{\overline{A}+\overline{B}}$ b)$\overline{\overline{\overline{ABC}}}$.
23. Solve the given Boolean equations using Boolean laws and deduce the truth table and circuit for the reduced equation and show the output of$\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C}$+A$\bar{B}\bar{C}$+ AB$\bar{C}$.
24. Solve the given Boolean equations using Boolean laws and deduce the truth table and circuit for the reduced equation and show the output of$\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C}$+A$\bar{B}\bar{C}$.
25. Solve the given Boolean equations using Boolean laws and deduce the truth table and circuit for the reduced equation and show the output of$\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C}$+ AB$\bar{C}$.

26. Reduce a) $\bar{A}\,\bar{B}C + \bar{A}B\bar{C}$+A$\bar{B}\bar{C}$+ A$\bar{B}C$ using K-Map and construct the circuit and show the output.
27. Reduceusing K-map b) $AB\bar{C}\bar{D} + AB\bar{C}D + ABCD + ABC\bar{D} + \bar{A}\,BCD + \bar{A}\,BC\bar{D} + \bar{A}\,B\bar{C}D$ and construct the circuit and show the output.
28. Reduce using K-map b) $AB\bar{C}\bar{D} + AB\bar{C}D + ABCD + ABC\bar{D} + \bar{A}\,BCD + \bar{A}\,BC\bar{D}$ and construct the circuit and show the output.
29. Reduce F(A,B,C)=∑m(0,1,5) using K-map and construct the circuit for the reduced equation and show the output.
30. Reduce F(A,B,C)=∑m(0,2,4,6) using K-map and construct the circuit for the reduced equation and show the output.
31. Reduce F(A,B,C,D)=∑m(0,1,4,5,9,13) using K-map and construct the circuit for the reduced equation and show the output.
32. Reduce F(A,B,C,D)=∑m(0,1,4,5,9,13) + d(3,7,11,15) using K-map and construct the circuit for the reduced equation and show the output.
33. Describe half adder circuits and write truth table, sum of products equation and implement using suitable logic gates.
34. Describe full adder circuits and write truth table, sum of products equation, reduce using K-map and implement using suitable logic gates.
35. Construct an adder circuit to add two bits with a possible carry from a lower column and write the truth table, sum of products equation, reduce using K-map and implement using suitable logic gates.
36. Construct a truth table to subtract two bits along with a possible borrow showing the difference and borrow results, write sum of products equation, reduce using K-map and implement the resulting full subtractor using suitable logic gates.
37. Illustrate the operation of IC 7483 for four bit binary addition.
38. Connect the circuit to implement the subtraction of two 4-bit data using IC 7483 using two's complement method.(use IC 7483 and IC 7486.) and show the output.
39. Develop Binary to Gray code converter using IC 7486 and verify the output.
40. Develop Gray to binary code converter using IC 7486 and verify the output.
41. Develop a 4-bit parity generator and checker using IC 7486.
42. Verify the truth table of 2-bit magnitude comparator using IC 7485.
43. Demonstrate an Enable/disable circuit using AND gates.
44. Demonstrate an Enable/disable circuit using OR gates.
45. Demonstrate an Enable/disable circuit using NAND gates.
46. Demonstrate an Enable/disable circuit using NOR gates.

End