Government of Karnataka
Department of Technical Education
Board of Technical Examinations, Bengaluru

Course Title :**Verilog Lab**		Course Code	: **15EC65P**
Semester	: **6**	Course Group	: **Core**
Teaching Scheme in Hr. (L:T:P)	: **0:2:4**	Credits	: **3**
Type of course	: **Tutorial + Practical**	Total Contact Hours	: **78**
CIE	: **25 Marks**	SEE	: **50 Marks**

Prerequisites

Knowledge of basic Mathematics, digital electronic circuits and Programming languages.

Course Objectives

Learn and understand the basics of Hardware description language and its use in designing electronic circuits.

Course Outcomes

At the end of the course, the students will be able to

1. Understand the basics of Hardware Description Languages, Program structure and basic language elements of Verilog.
2. Understand types of modelling, modules, functions of Verilog and simulate and synthesize related Programs.
3. Design, Simulate and synthesize various Verilog descriptions for Combinational circuits.
4. Design, Simulate and synthesize various Verilog descriptions for Sequential circuits.

Course Outcome		CL	Experiments linked	Linked PO	Teaching Hrs
CO1	Understand the basics of Hardware Description Languages, Program structure and basic language elements of Verilog.	***R/U/A***	Unit-1 Tutorial/practic e	1,2,3,4, 10	12
CO2	Understand types of modelling, modules, functions of Verilog and simulate and synthesize related Programs.	***R/U/A/ E***	Unit-1,Unit -2 E:1 to 2	1,2,3,4,5, 8,10	12+6=18
CO3	Design, Simulate and Synthesize various Verilog descriptions for Combinational circuits.	***U/A/E***	Unit -2, E:3 to 6	1,2,3,4,5, 8,10	15
CO4	Design, Simulate and Synthesize various Verilog descriptions for Sequential circuits.	***U/A/C***	Unit-2 E:7 to 11	1,2,3,4,5, 8,9,10	21
				Two CIE/IA Tests	06
				Student activity	06

Total sessions include two tests	**78**

Legend: R-Remember, U-Understand, A-Application, E-Evaluate, C-Create, CL-Cognitive Level, and PO-Program Outcome

Mapping Course Outcomes with Program Outcomes

Course Outcomes	Programme Outcomes									
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10
CO1	*	*	*	*	--	--	--	--	--	*
CO2	*	*	*	*	*	--	--	*	--	*
CO3	*	*	*	*	*	--	--	*	--	*
CO4	*	*	*	*	*	--	--	*	*	*

Course-PO Attainment Matrix

Course	Programme Outcomes									
	1	2	3	4	5	6	7	8	9	10
Verilog Lab	**3**	**3**	**3**	**3**	**3**	**--**	**--**	**3**	**1**	**3**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.
If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3
If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2
If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1
If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not addressed.

Course Contents

UNIT – 1: Tutorial and Practice — Duration: 24 Hrs.

Sl. No.	Topic/Exercises	Duration (Hr.)
1	Evolution of Computer-Aided digital design, Introduction to HDL, Importance of HDL, levels of abstraction, types of code-Structural and procedural.	3
2	Introduction to Verilog HDL, Definition, Program Structure of Verilog, **Lexical Tokens/Conventions**-explain with syntax-White Space, Comments, Numbers, Identifiers, Operators, Verilog Keywords. **Data types**-explain with syntax-Value Set, Wire, Reg, Input, Output, Inout Integer, Supply0, Supply1, Time, Parameter. Simple examples.	3
3	**Operators with examples**-Arithmetic, Logical, Relational, Bit-wise, Reduction, Shift, concatenation, Replication, Conditional operators. Operator Precedence.	3

4	**Operands**-explain with syntax-Literals, Wires, Regs, and Parameters, Bit-Selects, Part-Selects, Function Calls. Simple examples.	3
5	**Modules**-Module Declaration, Continuous Assignment, Module Instantiations, Parameterized Modules, Procedures: Always and Initial Blocks. Simple examples.	3
6	**Tasks and Functions**-display, strobe, monitor, reset, stop, finish etc. **Timing Control**-Delay Control(#), Events, wait Statement, join Statements.	3
7	**Behavioral Modeling**-Procedural Assignments, Delay in Assignment, Blocking Assignments, Non-blocking (RTL) Assignments, begin ... end, for Loops, while Loops, forever Loops, if ... else if ... else, disable, case. Simple examples.	3
8	**Functions**-Function Declaration, Return Value, Call, Function Rules, Simple Examples. Brief description about Gate-Level Modeling,Dataflow Modeling, Switch-Level Modeling.	3
	Total	**24**
	Practice Exercises	
	Write and execute verilog code for the following problems 1. Verilog Description for all two input basic gates. 2. Verilog Description for two input Arithmetic operations. 3. Verilog Description for three/four input Logical operations. 4. Compute the output for arithmetic expression. y=(a+b*c)/(a+c) 5. Compute the output for Logical expression. y= (A and B) or (B and C). 6. Verilog Description for 1-bit Full Adder 7. Verilog Description for 2:1 multiplexer using dataflow/behavioral method. 8. Verilog Description for 1:2 De-multiplexer using dataflow/behavioral method. 9. Verilog Description for 2-bit parallel adder. 10. Verilog Description for 2-bit ALU with any 2 arithmetic and logical operations. 11. Verilog Code for D-flipflop 12. Verilog Code for T-flipflop 13. Verilog Description for mod-6 counter.	

UNIT – 2: Graded Exercises Duration: 48 Hr.

Write the verilog code for the following problems and simulate using any HDL simulator/synthesis software (Xilinx/Modelsim/Simulink etc) and download to FPGA/CPLD trainerkits.

Sl. No.	Topic/Exercises	Duration (Hr.)
1	a) Verilog description for full-adder using structural modeling. b) Verilog description for full-adder using behavioral modeling.	3
2	Verilog description for 4-bit ripple carry full-adder using 1-bit full-adder.	3
3	a) Verilog description for BCD to seven segment decoder for common anode display using if else. b) Verilog description for BCD to seven segment decoder using case statement.	3

4	a) Verilog description for 4 -bit parallel adder. b) Verilog description for 4-bit comparator.	3
5	a) Verilog description for 4-bit ALU with three logical & three arithmetic operations. b) Verilog description for any three relational and three bit-wise operations.	3
6	a) Verilog description for 4-to-1 multiplexer using logic equations. b) Verilog description for 4-to-1 multiplexer using conditional operators. c) Verilog description for 4-to-1 multiplexer using behavioral modeling. d) Verilog description for 4-to-1 multiplexer using 2:1 muxes.	6
7	a) Verilog description for clocked T-flip flop. b) Verilog description for edge-triggered D-flip flop.	3
8	a) Verilog description for edge-triggered JK-flip flop. b) Verilog description for 4-bit counter using JK-flip flop.	6
9	a) Verilog description for BCD up/down counter using behavior modeling. b) Verilog description for 4-bit ripple carry counter using T and D-flip flop.	3
10	Verilog description for universal shift register.	3
11	Two open-ended experiments of similar nature as above are to be assigned by the teacher. Student is expected to solve and execute/simulate independently using verilog code.	6
	Two Internal Assessment Tests(CIE)	6
	Total Hours	**48**

Unit – 3: Student Activities [CIE- 05 Marks] 06 Hours & off-classes

Sl. No.	Activity	Duration (Hrs)
1	Develop the algorithm/flowchart and verilog description for the experiments as assigned by the teacher (Student is expected to solve and execute/simulate independently using verilog code). **E.g.**1.Design an 8-function ALU that takes 4-bit inputs A and B and a 3-bit input signal select, and gives a 5-bit output out. 2. Design 8:1 mux using two 4:1 mux. 3.Design the 4-to-1 multiplexer using if and else statements 4.Verilog code for 4 bit binary to gray converter. **Note**: 1.Teacher can assign one experiment per batch (<=4 students) for the student activity. 2. Prepare a Hand-written report of the above activity limited to 4 to 6 pages.	**06 Hrs & Off-class**

References

1. Fundamentals of Digital logic with Verilog design-2e, Brown Vranesic, McGrawHill education, ISBN-13:978-0-07-066724-2.
1. Verilog HDL-A guide to Digital Design and Synthesis-Samir Palnitkar-ISBN: 0134516753; Pub: Prentice Hall PTR.

2. Introduction to Verilog-.Peter M. Nyasulu.
3. Handbook on Verilog HDL-Dr. Daniel C. Hyde,Bucknell University
4. Verilog Tutorial – Deepak Kumar Tala
5. The Verilog Hardware Description Language-Donald Thomas and Philip Moorby (2008)
6. http://www.iitk.ac.in/eclub/summercamp/Courses/CompArch/Verilog_lab_Solutions.pdf
7. http://users.ece.utexas.edu/~ljohn/teaching/ee460m_lab_manual.pdf
8. http://treymorris.com/classes/elen/248/lab/lab%20manuals/lab_manual_5.pdf
9. http://d1.amobbs.com/bbs_upload782111/files_33/ourdev_585395BQ8J9A.pdf
10. www.cc.gatech.edu/~hadi/.../01.../verilog/An%20Introduction%20to%20Verilog.pdf
11. www.ece.niu.edu.tw/~chu/download/fpga/verilog.pdf
12. http://www.asic-world.com/
13. https://www.youtube.com/watch?v=QSEl_O0Gtoo&list=PLoM0uG7tqR3qVss3zhBRniXU7mhHy2bwj

Course Delivery

The course will be normally delivered through two-hour tutorials and four-hour hands-on practice per week; hands-on practice shall include verilog simulation programs. Normally, one-hour tutorial followed by two-hour hands-on practice is recommended in each class. Tutorial shall be imparted before the conduction of the experiment. However, activities are carried-out off-class and demonstration/presentation can be in lab sessions.

Course Assessment and Evaluation Scheme

Master Scheme

Assessment Method	What		To Whom	Assessment mode /Frequency /timing	Max. Marks	Evidence Collected	Course Outcomes
Direct assessment	CIE	IA	Students	Two tests+	**10**	Blue Books	1 to 5
				Record@	**10**	Record Book	1 to 5
				Activity*	**05**	Report/Sheets	1 to 5
	SEE	End exam		End of the course	**50**	Answer Scripts at BTE	1 to 5
				Total	**75**		
Indirect assessment	Student feedback on course		Students	Middle of the Course	Nil	Feedback Forms	1 to 3 & Delivery of course
	End of course survey			End of the Course	Nil	Questionnaires	1 to 5, Effectiveness of delivery instructions & assessment methods

Legends: CIE-Continuous Internal Evaluation, SEE- Semester End-exam Evaluation

[+] Every I.A. test shall be conducted as per SEE scheme of valuation. However, scored marks will be scaled down to 10. Average of two tests, by rounding off any fractional part thereof to next higher integer, shall be considered for IA.

*****Students should do activity as per the list of suggested activities/ similar activities with prior approval of the teacher. Activity process must be initiated well in advance so that it can be completed well before the end of the term. Rubrics to be devised appropriately by the concerned faculty to assess Student activities.

[@]Record Writing: Average of marks allotted for all experiments shall be considered; fractional part of average shall be rounded-off to next higher integer.

Composition of CLs

Sl. No.	Cognitive Levels (CL)	Weightage (%)
1	Remembering	20
2	Understanding	30
3	Applying	40
4	Evaluation	06
5	Create	04
	Total	**100**

Continuous Internal Evaluation (CIE) pattern

(i) Student Activity (5 marks):
The student activities in Unit-3 or similar activities can be assigned by the teacher

Execution Notes:
1. Each batch of 2 students is assigned at least one activity listed in Unit-3 based on interest of the students. Student can also choose any other similar /relevant activity with prior approval from the concerned teacher.
2. Teacher is expected to observe and record the progress of students activities
3. Assessment is made based on quality of work as prescribed by the following **rubrics** table

(ii) Model of rubrics for assessing student activity (for every student)

Dimension	Scale					Marks (Example)
	1 Unsatisfactory	2 Developing	3 Satisfactory	4 Good	5 Exemplary	
1. Information search and Collection.	Does not collect information relate to topic	Collects very limited information, some relate to topic	Collects basic information, most refer to the topic	Collects more information, most refer to the topic	Collects a great deals of information, all refer to the topic	3
2. Full-fills team roles and duties	Does not perform any duties assigned to the team role	Performs very little duties	Performs nearly all duties	Performs almost all duties	Performs all duties of assigned team roles	2

3. Shares work equality	Always relies on others to do the work	Rarely does the assigned work, often needs reminding	Usually does the assigned work, rarely needs reminding	Always does the assigned work, rarely needs reminding.	Always does the assigned work, without needing reminding	5
4. Listening Skills	Is always talking, never allows anyone to else to speak	Usually does most of the talking, rarely allows others to speak	Listens, but sometimes talk too much,	Listens and talks a little more than needed.	Listens and talks a fare amount	3
					Total marks	ceil(13/4)= 4

(iii) CIE/IA Tests (10 Marks)

Two tests shall be conducted in accordance with SEE pattern and the marks shall be scaled down to 10. Average of two tests, rounding-off any fractional part thereof to next higher integer, shall be considered for CIE/IA.

(iv) Record Evaluation (10 Marks)

Every experiment shall be given marks, in the scale of 10, after its conduction based on student's performance and quality of write-up. Average of them, by rounding-off any fractional part thereof to next higher integer, shall be considered for CIE/IA.

Semester End-exam Evaluation (SEE) Scheme

Sl. No.	Scheme	Max. Marks
1	Short questions onUnit-1 (only write-up)	05
2	Writing program and execution steps/procedure for two questions from the graded exercises.	20
3	Execution/Simulation of either one of the programs given in Sl. No. 2 above	15
4	Open-ended problem: Writing one program and its execution/implementation.	05
5	Viva-voce	05
	Total	**50**

Note:

1. Candidate is expected to submit record for the examination.
2. Student shall be allowed to execute the program even if she/he is unable to write the procedure/steps.
3. Open-ended problem is of the nature and magnitude similar to graded exercises in Unit-2, and it can be assigned by the examiner. Further, open-end programs executed in Unit-3 shall be excluded. Idea behind open-end program is to assess the ability of a student to write any program or creativity.

Model Questions for Practice and Semester End Examination

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N**ote:** The questions in the question bank are indicative but not exhaustive.

1. Write a verilog code for half-adder and full-adder using behavioral modelling.
2. Write a verilog code for half-subtractor and full-subtractor using behavioural modeling.
3. Write a verilog code for 4-bit full-adder, Using Dataflow Operators.
4. Write a verilog code for 4 bit parallel adder.
5. Write a verilog code for BCD to seven segment decoder.
6. Write a verilog code for 4 bit parallel adder.
7. Write a verilog codefor 4 bit comparator.
8. Write a verilog codefor 4-to-1 multiplexer, using logic equations.
9. Write a verilog codefor 4-to-1 multiplexer, using conditional operators.
10. Write a verilog codefor behavioral 4-to-1 multiplexer.
11. Write a verilog codefor1:4 de-multiplexer, using logic equations.
12. Write a verilog codefor1:4 de-multiplexer using behavioralmodeling.
13. Write a verilog code for clocked T-flipflop.
14. Write a verilog code for edge-triggered D-flipflop.
15. Write a verilog code for edge-triggered JK-flipflop
16. Write a verilog code forripple counter
17. Write a verilog code forbehavioral 4-bit counter.
18. Write a verilog code foruniversal shift register/left-right shifter using function.
19. Write a Switch-level verilogdescription of 2-to-1 multiplexer.
20. Write a Switch-level verilogdescription of CMOS inverter.
21. Write a Switch-level verilog for NOR-gate
22. Write a verilog code for 4-bit ALU with 3 logical & 3 arithmetic operations
23. Write a verilog code for any 2 relational and 2-bit-wise operations

End